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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,521	11/28/2001	Guenther Bergmann	4248	3542

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EXAMINER
SHINGLETON, MICHAEL B

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-996,521	Bergmann et al.
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 2-21-2002

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-7 and 11-13 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7 and 11-13 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)–(d)

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)–(d).

☒ All ☐ Some* ☐ None of the:

☒ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO–1449, Paper No(s). 4

☐ Interview Summary, PTO–413

☒ Notice of Reference(s) Cited, PTO–892

☐ Notice of Informal Patent Application, PTO–152

☐ Notice of Draftsperson's Patent Drawing Review, PTO–948

☐ Other _____

Office Action Summary

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: In a number of locations in the specification specific references to various claims are used for the description of the invention. Examples can be found on page 1 around line 6, page 2 around lines 11 and 14 for example. This is improper because the final numbering of the claims at time of issue could be different from that presented in the specification, and the claims can be amended during prosecution which would change the meaning of these passages which might raise issues of new matter, etc.. In fact note that page 2 around line 14 recites "features of patent claim 9", yet patent claim 9 has been cancelled by amendment dated 2-21-2002. Thus, this portion of the specification no longer has any meaning. Since there are many places that this appears it is requested of applicant to carefully check for any places the examiner may have missed.

Appropriate correction is required.

The abstract of the disclosure is objected to because the abstract should be a single paragraph. Correction is required See MPEP § 608.01(b).

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the memory unit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Naitoh 4,617,527 (Naitoh).

Figures 1 and 2 as well as the corresponding portions of the specification of Naitoh disclose a method for tuning a PLL (Phase Locked Loop) circuit 10 in which a control voltage A is generated from a phase detector 3 by way of a loop filter 4. Figures 1 and 2 of Naitoh also shows the PLL arrangement structure that is the subject of the claimed method for using the PLL i.e. "tuning". The control voltage A clearly determines the output frequency of the voltage-controlled oscillator 2. The output frequency from

the output of the VCO is feedback to the phase detector in the conventional manner such that the phase detector 3 inherently compares this feedback frequency with a desired frequency applied at input IN. Figure 2 and columns 1 and 2 of Naitoh specifically recites and shows a first mode where the control voltage A is increased until the output frequency of the VCO matches the desired frequency i.e. lock or the control voltage A reaches a first threshold value V_m (Note that Figure 2 shows the voltage increasing up to V_m at the end of the time period t_1 and note that if the lock detector 11 detected a lock before the reaching of the first threshold value this detection would cause the device to no longer be in the "first mode".) Figure 2 and columns 1 and 2 of Naitoh also specifically recites that shows a second mode where the control voltage A is decreased until the output frequency from the VCO matches the desired frequency (FR) i.e. lock or the control voltage A reaches a second threshold value V_n. (Note that Figure 2 shows the voltage decreasing to V_n at the end of time period t_2 and note that if the lock detector detected a lock before the reaching of the second threshold value this detection would cause the device to no longer be in the "second" mode.) If the second threshold value V_n is reached before lock then the device is switched into the first operating mode as is clearly illustrated by Figure 2. The lock detector 11 can be considered to be part of the phase detector 3 and this the phase detector (combination) would generate a control signal that indicates lock i.e. when the output frequency matches the desired frequency in that case there are no frequency dividers in the feedback path of the PLL. Elements that include elements 8, 9, G1, G2, 5 and 6 form at least one control unit that is linked to the loop filter and the phase detector as shown in Figure 1 of Naitoh that clearly monitors the control voltage of the VCO and compares the control voltage to the two threshold values as noted above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-7, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naitoh 4,617,527 (Naitoh) in view of Atriss et al. 5,285,114 (Atriss).

All the reasoning in the above rejection of claims 1 and 11 and the following: In conventional PLL's the control voltage applied to the VCO is modulated, i.e. changed, when the output frequency does not match the desired frequency and such is the case with Naitoh. Also as with the case of the conventional PLL with no frequency dividers in the feedback loop the control voltage is held constant when the PLL is in a locked state, i.e. the output frequency matches the desired frequency and such is the case with Naitoh. The phase detector of applicant is shown as a generic element (See Figure 1 of applicant's invention). The phase detector of Naitoh is also a generic conventional well-known phase detector and therefore the current of the phase detector of Naitoh inherently compensates for the currents used to charge-up or charge-down the filter which outputs the control voltage. At least this function is an obvious consequence of the combination made obvious herein. Likewise, since the phase detector of Naitoh is a generic conventional well-known phase detector like applicant's, the phase detector inherently supplies a temporally variable current to the loop filter the frequency of which is proportional to the size of the difference between the output frequency and the desired frequency. Naitoh utilizes voltage sources Vg and Vh along with the direction determining switches or switch 5,6 in combination with the specific filter to cause either an increase in the control voltage or a decrease in the control voltage. Naitoh does not employ current sources combined with a direction-determining switch in combination with a low pass filter to s to increase or decrease the control voltage. Naitoh does not show a memory means to store the operating state of the unit.

The method above is implemented by a device of Naitoh as noted above that includes a PLL (Phase Locked Loop) 10 having a phase detector 3 that is linked to a loop filter 4, and a VCO 2 connected to the loop filter in the conventional manner. The device also includes at least one control unit 20 that is connected to the loop filter and the phase detector 3 as is clearly illustrated in Figure 1. This control unit is also connected to the control voltage A and monitors this control voltage of the VCO. This device lacks a current source and current sink connected by means of a switching element so as to increase or decrease the control voltage A.

Figures 1 and 2 of Atriss disclose the use of a current source 30 to increase the control voltage, i.e. first mode of operation and a current sink 46 to decrease the control voltage, i.e. a second mode of operation These current arrangements are applied to a low pass filter to form a charge pump in the conventional manner and this provides exactly the same function as applicant's invention in that the control voltage is increased to increase the frequency output in a PLL and the control voltage is decreased

to decrease the frequency output in a PLL. Thus Atriss shows that the charge pump arrangement of Atriss is an equivalent structure known in the art. Therefore, because these two control voltage generating means were art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the charge pump arrangement of Atriss for the control voltage generation means of Naitoh. Furthermore, use of the charge pump arrangement of Atriss is recited as being advantageous for this charge pump is an improvement over other control voltage generating means for PLL's in that a linear charging current is obtained for the loop filter that is independent of loop voltage (See Column 1, around line 62). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the charge pump arrangement of Atriss for the control voltage generation means of Naitoh so as to obtain linear charging current that is independent of loop voltage.

As it relates to the limitation requiring the maximum amplitude of the current of the phase detector is greater than the amplitude of the current from the current source or the current sink and "the maximum amplitude of the current of the phase detector falls as the difference between the desired frequency and the output frequency increases" these merely represents the selection of the optimum or workable range and accordingly since the selection of these values involves but routine skill in the art the selection of these values would have been obvious to one of ordinary skill in the art at the time the invention was made. As to the use of memory to store the operating state of the unit, it is well known and conventional to use memory so as to store the operating states/conditions of circuits. Thus it would have been obvious to one of ordinary skill in the art to provide memory to the combination made obvious above since it was known in the art to use memory to store the operating state of a circuit which can be used among other things to adjust the circuit, determine the operating characteristics of the circuits, or used to set the operating conditions of the circuit upon start-up of the device. The obvious combination above includes a low pass filter and thus damping of the modulation amplitude of the control voltage by the low pass characteristic of the loop filter is an obvious consequence of the combination made obvious above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al and Inohana et al. Both disclose general state of the phase locked loops

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909 The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
July 22, 2003

MICHAEL B. SHINGLETON
PRIMARY EXAMINER